

Isaura S. Gaeta

*Fortune 50 Technology trailblazer experienced in scaling \$M products*

Sunnyvale, CA 408.656.1482 [lgaeta110@gmail.com](mailto:lgaeta110@gmail.com) [LinkedIn: Isaura-s-gaeta](https://www.linkedin.com/in/isaura-s-gaeta)

**Global technology executive, award-winning innovator and governance and manufacturing expert** who has driven large-scale, highly matrixed multi-billion-dollar R&D semiconductor product investments across multiple geographies—from prototype to high profile brand. Skilled at technical leadership and development.

- **Independent Director:** Member of the board of directors of Stearns Bank N.A., a private community bank and holding company.
- **Semiconductor Plant GM:** Rose to lead semiconductor facility after building deep expertise in technology development, NPI, manufacturing, yield improvement, quality, and safety. Ten-year track record of meeting State of California emissions and water requirements for the facility.
- **Operations:** COO-equivalent role overseeing 25K employees across multiple countries. Drove engineering strategy and execution with \$3B R&D budget for enterprise-wide data center, client and IOT product development.
- **Governance and Security Expertise:** Directs hardware security research across all Intel products. Initiated a company-wide security-first mindset and leads offensive security and physical attack engineering teams around the globe. Established external academic partner ecosystem.
- **M & A:** responsible for integration and divesting engineering teams into/from Intel corporation.
- **ESG:** Recognized thought leader and international speaker on diversity and inclusion in technology. Increased diverse engineering hiring by 50%. Sits on CEO level Executive Diversity Council at Intel.
- **Nonprofit Service:** Board Chair of the Hispanic Foundation of Silicon Valley, an organization dedicated to inspiring community philanthropy among the Hispanic community to improve quality of life for Latinos and the Silicon Valley region. Previously served on the boards of Women in Engineering ProActive Network and Stanford University El Centro Chicano y Latino Cultural Center.

#### Executive Experience

**Intel Corporation,** (NASDAQ: INTC) *Santa Clara, CA*

American semiconductor manufacturing company with \$79B+ in revenue (2021) and 120,000 employees.

**VP AND GM, SECURITY RESEARCH, INTEL PRODUCT ASSURANCE AND SECURITY GROUP,** 2018 – Present

Lead enterprise-wide security research across all Intel product lines. Drive research agenda to preempt fast-moving global cybersecurity threats, estimated to cost the world \$3T annually.

- **Risk Management:** Proactive research to address security threats or vulnerabilities prior to market, saving over \$100M per product family. Delivers Product security risk summary report to the BoD.
- **Security Champion:** Actively influences to build a security-first mindset into all phases of the product development lifecycle. Champions accountability with internal teams via an innovative report card. As a result, engineering has significantly improved hardware security design quality.

**VP AND GM, SYSTEMS ENGINEERING, PLATFORM ENGINEERING GROUP** 2017 – 2018

**CHIEF OF STAFF AND HEAD OF BUSINESS OPERATIONS, PLATFORM ENGINEERING GROUP** 2014 – 2017

Dual executive leadership roles for enterprise-wide engineering operations (COO equivalent). As Head of Business Operations, drove Technical Leadership Development, Risk & Controls, Ethics & Compliance, Audit, D&I, Communications, and operational adherence to \$3B R&D budget.

- **Operational Excellence:** Optimized capacity and quality management systems across 58 sites.
- **Product Delivery:** Achieved 90% of Intel's engineering deliverables, including stretch goals. Initiated E2E systems engineering between IP, Design and Validation teams to minimize gaps.
- **People Leadership:** Increased representation of women and minorities in engineering by 50%. Created Ethics and Compliance campaign resulting in 70% reduction in global violations in < 2yrs.
- **Systems Engineering:** Drove end-to-end workflow optimization to improve engineering efficiency and output across a global 25K-member operation from IP development to full Chip deployment.

**SENIOR DIRECTOR, CORPORATE AFFAIRS** 2009 – 2013

- **Corporate Responsibility:** Drove good corporate citizenship by excelling at environmental requirements, investing in local communities, and running global education programs to help get more women and underrepresented students into STEM fields around the globe.

**CO-GENERAL MANAGER FAB D2, CALIFORNIA TECHNOLOGY AND MANUFACTURING** 1984 – 2009

- Rose up the ranks to direct a 1,000-member silicon fabrication facility in California. Responsible for all aspects of operations and product output.
- Developed 8 new silicon technologies in addition to production volume.
- Safely decommissioned Si facility without any safety issues and reskilled workforce leading to high employee satisfaction despite closure.

### **Education and Certifications**

**Master of Science**, Electrical Engineering, **Stanford University**

**Bachelor of Science**, Electrical Engineering, **Stanford University**

Latino Leadership Institute Certificate, UCLA Anderson School of Management

National Association of Corporate Directors, Certificate in Risk Oversight and Management

National Association of Corporate Directors, Certificate in Compliance and Ethics

### **Recent Honors and Recognitions**

Class of 2021, 2020, 2019, 2018, 2017, 2016, and 2015 - Top 100 most influential and notable

Hispanic Professionals in Information Technology (HITEC 100)

December 2022 Womentech Global Awards 2022 Keynote Speaker

April 2021 featured in Hispanic Executive Magazine Leading Latinas issue

April 2021 featured speaker at Advancing Women in Technology (AWT) event

2020 - 60 Technical Women Leaders: The Next FORTUNE 500 CTOs – Girl Geek X

2018 Top Latino Leaders award issued by National Diversity Council

2016 *The Alumni Society* Class of 2016 Hispanic Leaders in America

Global keynote: Perspektywy Women in Tech Summit 2019 Poland